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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/782,090	02/12/2001	Mordechai Daniel	P-181-1 US	9723

23366 7590 11/10/2003

MORTON CHIRNOMAS & ASSOC.  
11355 W. OLYMPIC BLVD.  
SUITE 100  
LOS ANGELES, CA 90064

EXAMINER

NGUYEN, TANH Q

ART UNIT	PAPER NUMBER
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2182

DATE MAILED: 11/10/2003

6

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/782,090

Applicant(s)

DANIEL ET AL.

Examiner

Tanh Q. Nguyen

Art Unit

2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) 20-33 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 February 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. 6) ☐ Other:

**DETAILED ACTION**

***Election/Restrictions***

1. Applicant's election with traverse of claims 1-19 in Paper No. 5 is acknowledged. The traversal is on the ground(s) that "Regarding groups I and II, computer systems do generally have a CPU and therefore the Examiner's comment seems unreasonable" and that "Applicant believes that a generic claim can be drawn to the system to provide adequate coverage". This is not found persuasive because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement.

Applicant did not provide any evidence that the apparatus as claimed can only be used to practice only one process, or one process and another process that is not a materially different process than the one process; any evidence that the process(es) as claimed can only be practiced by the apparatus claimed; and any evidence that the subcombinations are not separately usable.

Further, regarding groups I and II, the invention is not directed to only computer systems having a CPU. Rather, Group I is directed to a computer system for transferring data between a receiving CPU and a transmitting CPU by using only write operations, and Group II is directed to a method for writing a data message into a receiving queue. Still further, there is no generic claim in the pending claims (1-33).

The requirement is still deemed proper and is therefore made FINAL.

2. Claim 32 link(s) inventions I and II. Claim 33 link(s) inventions I and III. The restriction requirement between the linked inventions is subject to the nonallowance of the linking claims, claim 32 and claim 33. Upon the allowance of the linking claims, the

restriction requirement as to the linked inventions shall be withdrawn and any claim(s) depending from or otherwise including all the limitations of the allowable linking claim(s) will be entitled to examination in the instant application. Applicant(s) are advised that if any such claim(s) depending from or including all the limitations of the allowable linking claim(s) is/are presented in a continuation or divisional application, the claims of the continuation or divisional application may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Where a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. *In re Ziegler*, 44 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

3. Claims 20-31 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Claims 32-33 are also withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim – as claim 32 includes all the steps of claim 20 (Group II) and claim 33 includes all the steps of claim 26 (Group III). Claim 32 would be <sup>considered</sup> allowable if claim 1 is allowable, and claim 33 would be <sup>considered</sup> allowable if claim 12 is allowable. Applicant timely traversed the restriction (election) requirement in Paper No. 5.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

### ***Specification***

5. Claims 18-19 are objected to because of the following informalities: claims 18-19 made reference to a “magic” number contained in a message stopper, without defining what the magic number is - when it is contained in the message stopper. The specification discloses that the magic number is used to check for validity ([0044] of US 20020112105 A1) when it is contained in a message separator (not a message stopper). The examiner, therefore, interpreted the magic number in the message stopper as being the same as the magic number in the message separator. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for using “faster write operations across the PCI bus...to take advantage of the relative speed of writes in a PCI system” (Abstract, lines 6-8), does not reasonably provide enablement for “using only write operations” (claim 1, lines 2-3). The specification does not enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. It appears that read operations are performed within the transmitter [210, FIG. 2] and within the receiver [200, FIG. 2].

8. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The registers required for a write operation across the PCI bus, critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The limitations of claim 1 would not support a data transfer between a receiving CPU and a transmitting CPU using only write operations (across a PCI bus) without the registers being configured for write only operations across the PCI bus. The limitation "by using only write operations" further does not carry any patentable weight for the same reason.

9. Claims 2-19 are rejected because they depend on claim 1.

10. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a total write register [270, FIG. 2], does not reasonably provide enablement for the total write register being in the receiving memory. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. It appears that the claim should recite in lines 1-2, "said transmitting memory further comprises a total write register".

11. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a transmitting total read register [260, FIG. 2], which contain a second copy of the total quantity of data read from the queue by the receiving CPU, does not reasonably provide enablement for the transmitting total read register being in the receiving memory. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. It appears that the claim should recite in lines 1-2, "said transmitting memory further comprises a transmitting total read register".

12. Claim 14 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a message separator containing the length of a message, does not reasonably provide enablement for a message separator that is used to indicate the end of said message to also contain the length of the same message. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. As understood by the examiner, the message separator that is used to indicate the end of the message is also used to indicate the length of the immediately following message.

13. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. Claim 1 recites the limitation "second CPU" in line 8 without "a first CPU". There is insufficient antecedent basis for this limitation in the claim.

Further, "second CPU" would have suggested a CPU that is neither the transmitting CPU, nor the receiving CPU. If this is the case, the limitation "second CPU" would not be appropriate. Appropriate correction is required.

16. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the registers required to effect the data transfer between a receiving CPU and a transmitting CPU by using only write operations (across the PCI bus).

17. Claim 1 provides for the use of only write operations, but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

Claim 1 is rejected under 35 U.S.C. 101 because the claimed recitation of a use, without setting forth any steps involved in the process, results in an improper definition of a process, i.e., results in a claim which is not a proper process claim under 35



U.S.C. 101. See for example *Ex parte Dunki*, 153 USPQ 678 (Bd.App. 1967) and *Clinical Products, Ltd. v. Brenner*, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966).

18. Claims 2-19 are rejected because they depend on claim 1.

19. Claim 8 recites the limitation "said at least one control register in said receiving memory" in lines 1-2. Claim 8 also recites the limitation "a second copy" in line 3 without "a first copy". There is insufficient antecedent basis for the above limitations in the claim.

20. Claim 10 recites the limitation "said pointer for the next write" in line 2. There is insufficient antecedent basis for the above limitations in the claim. Claims 10-19 are rejected because they depend on claim 10.

21. Claim 11 recites the limitation "said message" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. Claim 11 is also indefinite, as "a maximum length is specified for said message" does not clearly indicate that a maximum is imposed on the length of the message. Claims 12-19 are rejected because they depend on claim 11.

22. Claim 12 is indefinite as "a tail is added at the end of said queue equal to said maximum length for said message" does not clearly indicate that the tail has a length that is equal to the maximum length imposed on a received message. Claims 13-19 are rejected because they depend on claim 12.

***Claim Rejections - 35 USC § 102***

23. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

24. Claims 1-8 are rejected under 35 U.S.C. 102(a) and 102(e) as being anticipated by **Daniel et al. (USP 6,115,761)**.

25. As per claim 1, **Daniel et al.** (Daniel) teaches a computer system [FIG. 5] for transferring data between a receiving central processing unit (CPU) and a transmitting CPU by using only write operations (col. 8, lines 32-33), comprising:

- i) at least one receiving CPU [12, FIG. 5];
- ii) at least one transmitting CPU [22, FIG. 5];
- iii) a local memory for receiving CPU [18, FIG. 5];
- iv) a local memory for transmitting CPU [SHARED MEMORY in 20, FIG. 5];
- v) means [30, FIG. 5] for connecting between receiving CPU and second CPU [22, FIG. 5] where such means transfer write operations faster than read operations (col. 4, lines 34-35); and

vi) a circular queue [50, FIG. 5; FIGs. 3E-3F, 4E-4F; col. 3, lines 31-32] defined between designated addresses in said local memory of said receiving CPU.

26. As per claims 2-8, Daniel teaches at least one receiving control register [52, 54, FIG. 5] for control of said queue, allocated in said local memory of said receiving CPU – claim 2;

at least one register [56, 58, FIG. 5] for control of said queue, said at least one register being allocated in said local memory of said transmitting CPU – claim 3;

said means for connecting between said CPUs being a PCI bus (col. 4, line 40) – claim 4;

the at least one control register in said receiving memory being a receiving total read register [54, FIG. 5], which contains a first copy of the total quantity of data read from said queue by said receiving CPU - when the total quantity of data read from said queue by said receiving CPU is less than the length of the queue – claim 5;

the at least one control register in said receiving memory further comprising a receiving total write register [52, FIG. 5], which contains the total quantity of data written into said queue of said receiving CPU by said transmitting CPU- when the total quantity of data written into said queue of said receiving CPU, by said transmission CPU is less than the length of the queue – claim 6;

the at least one control register in said transmitting memory further comprising a write head register [56, FIG. 5], which contains a pointer to the location of the next write into said queue – claim 7;

the at least one control register in said transmitting memory further comprising a transmitting total read register [58, FIG. 5], which contains a second copy of the total quantity of data read from said queue by said receiving CPU - when the total quantity of data read from said queue by said receiving CPU is less than the length of the queue – claim 8.

***Claim Rejections - 35 USC § 103***

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

28. Claims 9-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Daniel et al.**.

29. As per claim 9, Daniel teaches the limitations of claim 2 and said at least one control register in said receiving memory further comprises a read head register [54, FIG. 5], which contains a pointer to the location of the next read from said queue. Daniel, therefore discloses the invention except for the at least one control register in said receiving memory being a receiving total read register, which contains a first copy of the total quantity of data read from said queue by said receiving CPU.

Since it was well known in the art at the time the invention was made to use a total read register (which contains a total quantity of data read from a queue) and a total

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write register (which contains a total quantity of data written to a queue) in a memory to monitor the status of the queue in the memory, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a receiving total read register and a receiving total write register in the receiving memory to monitor the status of the queue in the receiving memory (especially for a queue with more than one read pointer and/or more than one write pointer).

30. As per claim 10, Daniel teaches the pointer for the next read from the queue and the pointer for the next write into the queue being set to point to the same address upon initialization [FIG. 3A, FIG. 4A].

31. As per claim 11, Daniel teaches the queue being applied to any multiprocessor system (col. 11, lines 52-59), hence encompasses systems processing messages. Since it was well known in the art at the time the invention was made to impose a maximum message length to messages written into a given queue to improve queue management, it would have been obvious to one of ordinary skill in the art at the time the invention was made to impose a maximum message length to messages written into Daniel's queue to improve queue management.

32. As per claim 12, since it was well known in the art at the time the invention was made to add a tail at the end of a circular queue, the tail having a length equal to the maximum message length to improve queue performance, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add such a tail at the end of Daniel's queue to improve its performance.

33. As per claims 13-14, a message in a queue system inherently includes a separator that is used to indicate the end of a message and a message separator that contains the length of the message.

34. As per claims 15-16, since it was well known in the art at the time the invention was made to provide a valid indicator with a message to ensure proper processing of the message, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include such indicator into the message separator to ensure proper processing of Daniel's messages.

35. As per claims 17-19, since it was well known in the art at the time the invention was made to use a stopper to mark the end of the last message in a queue and message separators to mark separation between messages, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a stopper to mark the end of the last message in Daniel's queue.


36. Claims 9-19 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over **Daniel et al.** in view of **Young et al. (USP 6,006,292)**.

**Young et al.** (Young) teaches a total read register [132, FIG. 1] which contains a total quantity of data read from a queue, a total write register [131, FIG. 1] which contains a total quantity of data written to a queue to monitor the status of the queue in the memory of the host adapter, and a read pointer [156, FIG. 1] to the location of the next read from the queue. See rejections 9-19 over Daniel above for basis of rejections.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (703) 305-0138, and whose e-mail address is [tanh.nguyen36@uspto.gov](mailto:tanh.nguyen36@uspto.gov). The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin, can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 for After Final, Official, and Customer Services, or (703) 746-5672 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

  
JEFFREY GAFFIN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100

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October 31, 2003